Lec 21-22 part 1

Lec (10) المحاضرة الأخيرة Semiconductor devices

FET

FET.. field effect Transistor

→ The current flow between the two terminal (source S & Drain D) is controlled by an electric field applied to the third terminal (gate G).

→ FET is called (Unipolar) because current depends only on majority carriers (e or h) = one carrier only. while NPN or PNP depends on 2 carriers.

→ **Advantages & disadvantages of FET compared to BJT**

مزايا

1- FET is Voltage controlled current source Device (VCCS) while BJT is current controlled current source ~ (CCCS).

2- FET has large i/p impedance, so it is pereffered than BJT as input stage to multistage amplifier

3- FET generates lower noise level than BJT.

4- FET more Temperature stable than BJT.

5- FET is easier to be fabricated than BJT

6- FET act as VCR (voltage controlled resistor)

عيوب disadvantages

1- FET has poor frequency response (low BW)

2- Poor linearity (non linear relation between I_D, V_{GS})

3- Due to static charges → Damage occured.

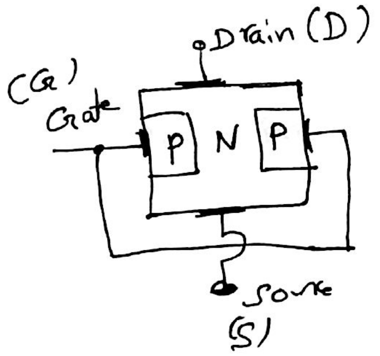
→ Uses of FET → Flashmemory, USB drive, Camera, laptop, cpu, -- etc

Transistor Family

- Fieldeffect Transistor
  - junction FET
    JFET
    - Depletion Mode
      - N-channel
      - P-channel
  - Metaloxidesemiconductor fet
    MOSFET
    - Depletion mode
      - N-ch
      - P-ch
    - Enhancement mode
      - N-ch
      - P-ch
- Bipolar junction Transistor
  (BJT)
  - NPN
  - PNP

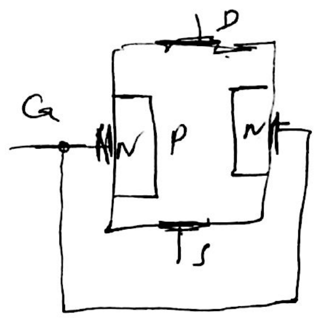
$\boxed{1}$ JFET (junction Field effect Transistor)

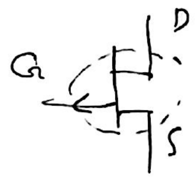
1- N-channel



Symbol

2- P-channel





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- it is a 3 terminals semiconductor devices, The current conduction by one type of carriers (Electrons, holes)

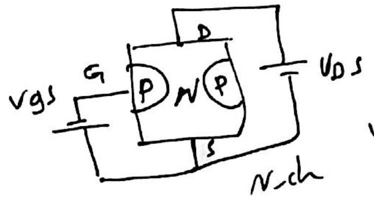
- Uses of FET more than BJT. (Nowdays)

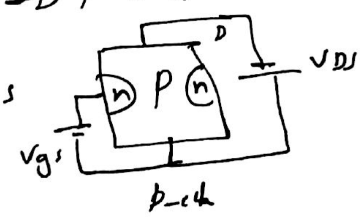
Notes (Operation of JFET)

[1] The voltage between gate and Source (gate Reverse biased)

[2] The input circuit (gate-to-Source) of JFET is reverse biased
∴ device has high input impedance.

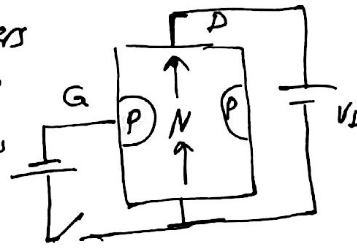
[3] The drain is so biased with respect to Source, So I_D pass (flow) From Source to drain.





[4] in All JFETs, $I_S = I_D$

Working



[1] The two PN junction at the sides From depletion Layers
The current conduction by charge carriers (free electrons) flow through the channel between the 2 depletion layers & out of the drain.

[2] the width of this channel (Resistance) can be controlled by changing The input voltage (V_{GS})

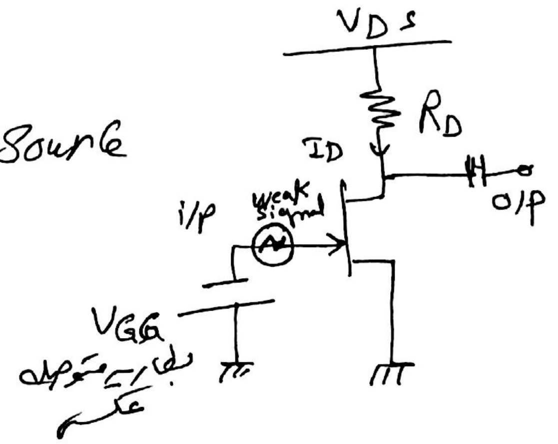
If V_{GS} ↑↑ → depletion region (wider) → Conduction channel (Narrower)

[3] JFET operates on principle That width of & hence Resistance of Conducting channel can be varried by changing $\underline{V_{GS}}$

OR [the magnitude of Drain Current I_D changed By V_{GS}]

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

JFET as amplifier



* a weak signal applied between gate & source & amplified output obtained in the Drain source circuit.

* VGG reverse connected with weak signal

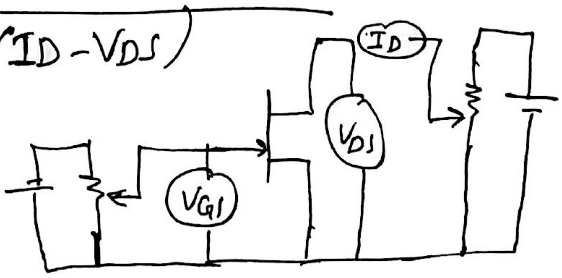
* A small change in the reverse Bias on gate → Produce large change in I_D.

1// * During ~~Positive~~ negative half cycle of the signal, the reverse voltage on gate increases & I_D decreases → The result is small change in voltage at the gate large change in drain current. (I_D)

2// * during Positive half cycle → The reverse bias on gate decrease This increase channel width & increase drain current.

3// * Now, large variation of drain current → Produce output across load R_D ⟶ so FET act as an amplifier

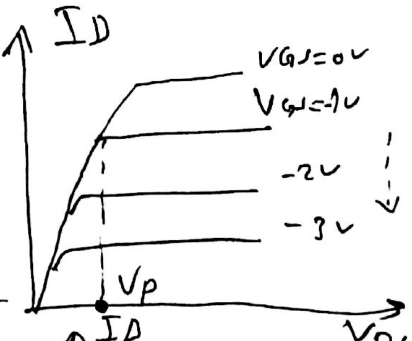
output characteristics of JFET (I_D-V_{DS})



* firstly, I_D increased rapidly with V_{DS} ↑ but then become constant. (where $V_{DS} = V_p$ pinchoff)

* after V_{DS} increased than V_p, the channel width become narrow, depletion region touch each other, I_D passes through small area between these layers ∴ The increase of I_D is very small with ($V_{DS} > V_p$) ∴ I_D remains constant

o/p ch/c



(JFET)